Optical-Logic-Gate Aided Packet-Switching in Transparent Optical Networks

Hassan Teimoori, Dimitrios Apostolopoulos, Kyriakos G. Vlachos, *Member, IEEE*, Cédric Ware, *Member, OSA*, Dimitrios Petrantonakis, Leontios Stampoulidis, Hercules Avramopoulos, and Didier Erasme

***Abstract*—The objective of this research is to propose two new optical procedures for packet routing and forwarding in the framework of transparent optical networks. The single-wavelength label-recognition and packet-forwarding unit, which represents the central physical constituent of the switching node, is fully described in both cases. The first architecture is a hybrid opto-electronic structure relying on an optical serial-to-parallel converter designed to slow down the label processing. The remaining switching operations are done electronically. The routing system remains transparent for the packet payloads. The second architecture is an all-optical architecture and is based on the implementation of all-optical decoding of the parallelized label. The packet-forwarding operations are done optically. The major subsystems required in both of the proposed architectures are described on the basis of nonlinear effects in semiconductor optical amplifiers. The experimental results are compatible with the integration of the whole architecture. Those subsystems are a 4-bit time-to-wavelength converter, a pulse extraction circuit, a an optical wavelength generator, a 3×8 all-optical decoder and a packet envelope detector.**

***Index Terms*—Optical header processing, optical logic gate, optical packet switching, semiconductor optical amplifier (SOA), transparent optical network.**

I. Introduction

In order to cope with the rapid growth of IP traffic, the optical network is becoming an important part of global telecommunications infrastructure. At present, the huge capacity of optical fibers in wavelength division multiplexing (WDM) transmission schemes is not employed optimally as a consequence of the electronics bottleneck at the network nodes. However, transparent networking remains a hot research subject, which aims to address various issues such as computational power, storage capacity, real-time processing, inflexibility of configuration, and network level cost.

Manuscript received November 8, 2007; revised March 10, 2008. Current version published October 24, 2008. This work was supported in part by the ePhoton/ONe+ project.

H. Teimoori, C. Ware, and D. Erasme are with Institut TELECOM/TELECOM ParisTech-Ecole Nationale Supérieure des Télécommunications, 75634 Paris, France (e-mail: teimoori@site.uottawa.ca; ware@enst.fr; cedric.ware@telecom-paristech.fr; didier.erasme@telecom-paristech.fr).

D. Apostolopoulos, D. Petrantonakis, L. Stampoulidis, and H. Avramopoulos are with National Technical University of Athens, Zografou, GR 15773, Athens, Greece (e-mail: apostold@mail.ntua.gr; petranto@mail.ntua.gr; lstamp@mail.ntua.gr).

K. G. Vlachos is with Computer Engineering and Informatics Department and Research Academic Computer Technology Institute, University of Patras, Rio 26500, Greece (e-mail: kvlachos@ceid.upatras.gr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JLT.2008.925065

Among the network switching strategies, burst-switching is more compatible with the current state of optoelectronic technology in terms of data transparency and switching speed. Nevertheless, optical packet-switching is more efficient for WDM data communication, but, due to the limited speed on electronics (in comparison with the available optical bandwidth in fiber optics) and the insufficient evolution of all-optical signal-processing alternatives, packet-based optical networks are not yet a practical solution for the implementation of transparent optical networks.

In packet-switching, the packets are steered towards their destinations by interrogating their destination address encoded in their header (which will be called "label" in this paper as a reference to the MPLS protocol). The packet label must be separated, recognized and possibly rewritten in every core router. This can be time consuming given that core routers have to forward millions of packets per second. As most core routers in backbone or metro networks have only four to eight outgoing ports, it may be possible to determine a packet's outgoing port by looking at only a small subset of the label bits in the destination address and thus the cost and complexity of individual components of the all-optical label-switching node can be reduced. The central part of a WDM packet-switching node is the single-wavelength (possibly waveband) label-recognition and packet-forwarding unit. This unit is to be inserted in a complete switching matrix as described for example in [1]. The total number of single-wavelength switches is equal to the product of the number of input fibers times the number of wavelength per fiber. "Add-fiber-channels" and "contention feedback-delays-line channels" [2] (if used) are to be counted as input fibers. The number of output fibers (including drop-fiber-channels and feedback-delay-line-fiber-channels) is limited by the physical characteristics of the switch elements.

The label and the payload transmission parameters (in terms of bit rate, wavelength and modulation format) are not necessarily the same since they can be processed separately. Four main approaches have been proposed for optical label coding: wavelength-labeling, subcarrier multiplexing (SCM), optical orthogonal modulating, and bit-serial-labeling. Each method has some specific advantages and disadvantages [3]. However, the main concern lies in the compatibility of the method with the various elements of the routing system. The bit-serial approach is used in the architectures described in this article. There, both the label and payload are modulated with the same format and at the same bit-rate in order to simplify the emission hardware and software. This reduces not only the packet format complexity, but also the label duration (leading to a greater effective data rate).

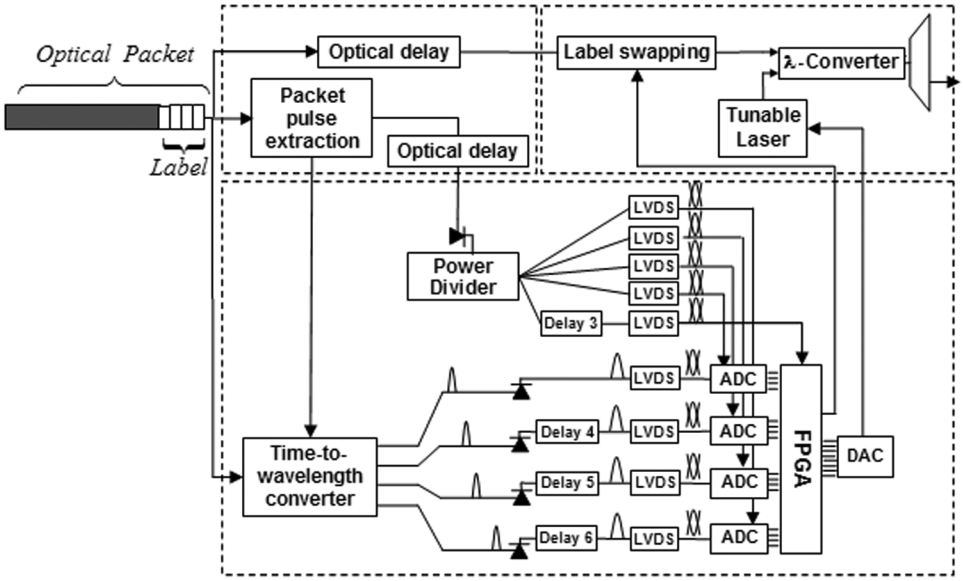


Fig. 1. Schematic diagram of the proposed optoelectronic packet-switching system.

During the past few years, a number of header recognition strategies dedicated to optical packet-switching have been proposed. The methods reported in literature can be categorized as interferometric methods [4], bit-pattern matching methods [5], slowed-down label processing [6] and all-optical self-routing methods.

Interferometric methods are based on the autocorrelation of the packet label sequence. They are limited to specific label sequence coding similar to those encountered in CDMA systems. Bit-pattern matching methods consist in comparing every input packet label with some pre-stored bit-patterns. Here, generating the label bit-patterns is mandatory, complex and costly.

In this paper, we present two new slowed-down label processing method in Sections II and III, respectively. Slowed-down label processing consists in reducing the data rate of the label so that it can be easily processed. All-optical "slowing down" process is demonstrated. This is particularly important in the case of optoelectronic processing of the label (as in Section II) since it allows usage of reduced speed (reduced cost) electronics. In all-optical solutions (Section III) the slow-down operation facilitates the label processing. Both architectures are transparent for the payload data. In order to simplify the requirements in all-optical packet-switched networks and to eliminate the need for an optical address lookup table, a new self-routing technique will be presented in Section III in which the allocated time for packet-label-processing and packet-routing can be reduced via all-optical solutions. The key objective in designing our all-optical packet-switching architecture is to develop an efficient and transparent packet-forwarding method using an optical label-switching mechanism.

II. Optoelectronic Packet-Switching System

Our first proposal for packet-switching node architecture is the optoelectronic packet-switch presented in Fig. 1. The proposed architecture includes three main subsystems: synchronization and buffering, label extraction and processing, and packet forwarding. In this section, we present these subsystems in detail. The number of bits in the label that can be extracted sets a limit to the number of output ports (fibers). The main limitation is here the time-to-wavelength unit described in Section II-B, which was demonstrated for operation on 4 bits, i.e., 16 addresses at 10 Gbit/s, which is probably more than needed for a core-network node. Contention may occur when two or several packets arrive at the same time (or overlap in time) from different input fibers and aim toward the same output port with the same wavelength (imposed by the active switch). (No contention occurs for packets arriving from the same fiber aiming towards the same output fiber since they are converted to different wavelengths). In the case of contention, the extra packet(s) can be directed toward one(several) contention delay-line fiber(s) or toward an other node if nothing else is possible. These solutions are fully analyzed in [2]. The contention control information is available via the FPGAs in each routing node. Another contention resolution scheme using feed-forward buffers is summarized in Section II-C [7]. It is much less demanding on information required by the control unit and is therefore compatible with the all-optical switches, which cannot provide all the information required otherwise (as in [1] or in Section III of this paper).

A. Synchronization and Buffering

The contribution of the synchronization and buffering subsystem is twofold; first, it conserves the packet payload information in the optical domain during the processing and packet-routing operations performed on the packet label, and second, it is responsible for timing and synchronizing the different subsystems. Thus, the packet-label coding format and the packet buffers must be compatible with the characteristics of all the other subsystems.

1) Determination of Packet Arrival Times: Most of the current clock recovery systems use a fast photo-detector followed by an electrical clock recovery. Optoelectronic alternatives or

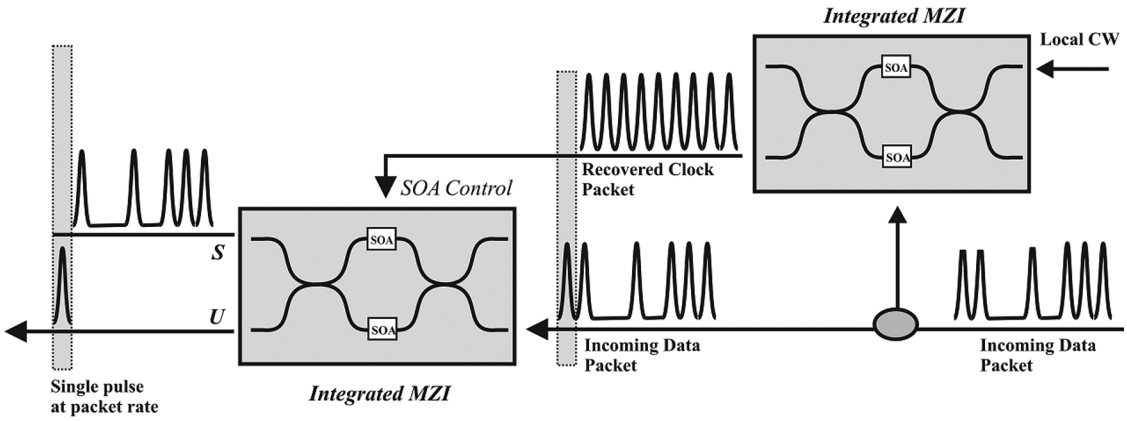


Fig. 2. Single pulse-extraction circuit.

all-optical solutions have difficulties in coping with the burst nature of packet transmission. In our design, a true clock recovery is not an absolute requirement. Only the beginning of each packet must be known. Provided that there is a marker pulse at the beginning of the packet in the form of either wavelength, polarization, bit period or amplitude, a packet pulse-extractor subsystem can serve for determining the packet arrival time with the required accuracy.

The proposed scheme is illustrated in Fig. 2. It comprises a packet clock recovery circuit [8] in order to provide the packet clock signal and an optical AND-gate to extract the first pulse of the packet identifying its beginning. The clock recovery module employs a Fabry-Perot Filter (FPF) and a hybrid SOA Mach-Zehnder Interferometer (SOA-MZI). The packet clock-recovery circuit requires two consecutive "1"s at the beginning of each packet in order to acquire the clock and decays within 15 bits. A second SOA-MZI switch is dedicated to the extraction of the first pulse of the packet. The incoming packet is logically ANDed with the locally generated packet clock signal delayed by a single bit. In this way, the first pulse appears in the unswitched port (U) of the MZI and is separated from the rest of the packet, which appears in its switched port (S).

The circuit has been evaluated with 10-Gbit/s PRBS $2^7 - 1$ synchronous and asynchronous data packets of variable length. Typical results are shown respectively in the left and right columns of Fig. 3. Fig. 3(a) depicts the leading part of the input data packet from a synchronous packet sequence and a sequence of two asynchronous packets. Fig. 3(b) shows the corresponding recovered clocks at the output of the clock recovery module. The packet clock-recovery circuit requires two consecutive "1's at the beginning of each packet in order to acquire the clock and decays within 15 bits. Fig. 3(c) and (d) shows the corresponding extracted first pulse(s) synchronization signals and the respective eye-diagrams at the output of MZI 2. The extinction ratio at MZI 2 between the extracted pulses and the following packet bits was in excess of 10 dB.

2) Optical Buffer: A fiber delay line (FDL) is a simple solution for optical buffering through which the departing times of packets are time-shifted. However, they can only provide limited buffer capacity and coarse delay granularity due to the bulky size of FDL [9]. Slow light techniques are also proposed for optical buffering applications [10].

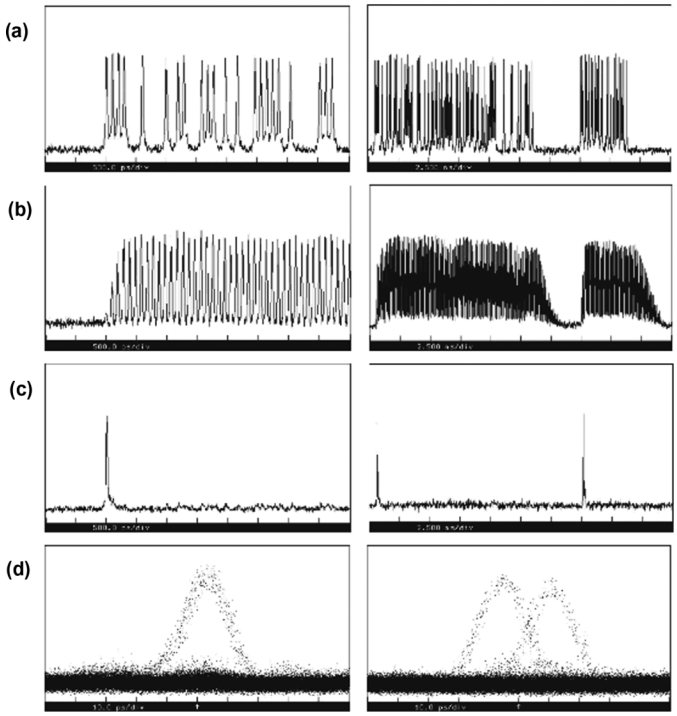


Fig. 3. Oscilloscope traces; Left column: synchronous operation (time scale 500 ps/div), right column: asynchronous operation (time scale 2.5 ns/div). (a) Input data packets. (b) Recovered clock packets. (c) Packet-rate synchronization pulse stream. (d) Eye diagrams (time scale 10 ps/div).

B. Label Extraction and Processing

The basic idea relies on time-to-wavelength conversion whereby a subset of a packet label is distributed onto distinct wavelengths. In other words, the time-to-wavelength converter serves as a serial-to-parallel converter. Then the parallelized bits are processed within an electronic signal processing subsystem in order to deliver the proper command signals to the optical-payload switch, to the contention control unit and to the label-swapping subsystem.

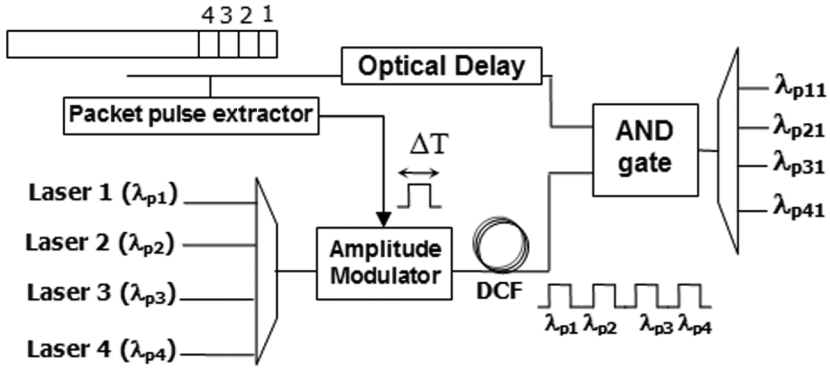


Fig. 4. Schematic diagram of a 4-bit time-to-wavelength converter.

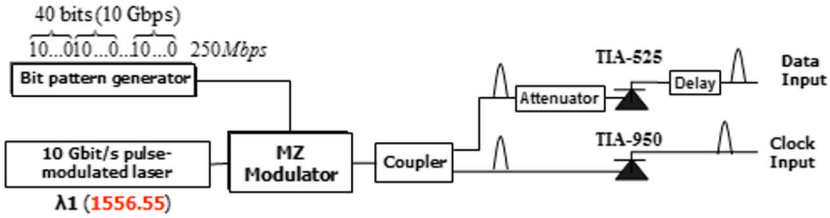


Fig. 5. Experimental set-up used for generating the input and clock pulses required for the test the LVDS and ADC circuits.

1) Label Extraction: A four-bit time-to-wavelength converter has demonstrated in an earlier experiment at 10 Gbit/s (see Fig. 4) [11]. Each consecutive bit of optical serial data sequence interacts with a single bit pulse carried on one of four distinct auxiliary wavelengths. In order to obtain the required overlap, the amplitudes of four auxiliary lasers multiplexed on a single optical fiber are modulated by a single pulse (generated by the pulse packet-extraction subsystem) of a duration smaller than or equal to the label bit-time and delayed with respect to one another in a dispersive element [here a dispersion compensating fiber (DCF)].

The results of four-bit time-to-wavelength conversion based on the four wave mixing (FWM) effect in a SOA were presented in [11]. The data sequence (probe) at $\lambda = 1553.1$ nm is launched together with 4 auxiliary modulated beams (pump) at $\lambda = 1551.4$ nm, 1550.95 nm, 1550.15 nm, and 1549.35 nm. The maximum modulating pulsewidth is 100 ps for a data sequence of 10 Gbit/s. The modulator is a Mach-Zehnder $LiNbO_3$ device and the DCF has 2.4 km long. The probe and pump powers in the SOA input are -7.6 and -3.7 dBm, respectively. The extinction ratio is between 9 and 12.5 dB. In all four cases, the signal amplitudes are different for each wavelength due to different FWM frequency detuning. A time-to-wavelength converter, which enhances polarization insensitivity, has also been demonstrated at 10 Gbit/s. Furthermore, it can be argued that this setup is easily modified in order to cope with higher bit rates.

2) Label Processing: The parallelized time-to-wavelength converter output bits exits the converter with fixed delays (100 ps at 10-Gbit/s bit-rate in the previous design). These delays can be easily compensated, either optically or electrically.

By means of four photo-detectors, the parallelized bits are converted into electrical format. Next, they are transformed into the low-voltage differential signaling (LVDS) format before processing. Low-voltage power supply compatibility, low noise generation, high noise rejection, high data rates ranging up to 2 Gbit/s, robust transmission signals, and ability to be integrated into system level ICs are other benefits of LVDS technology. LVDS uses a dual wire system, running with a π-phaseshift with respect to one another. A wideband transformer, such as Mini-Circuits ADT1-1WT (0.4–800 MHz), can provide the differential analog inputs for connecting the photo-detector output on the ADC input.

An 8-bit Analog Devices AD9480 analog-to-digital converter (ADC) optimized for a 250 MSPS conversion rate is used for sampling, amplifying and buffering the electrical analog bits as well as producing a variable detection threshold level. The configuration presented in Fig. 5 is used for generating the input and clock pulses in order to test the LVDS and ADC circuits. As the packet pulse extractor is used in several subsystems (e.g. ADCs' chip enable and FPGA) it is amplified via an electrical amplifier.

Fig. 6 displays the inputs and output of the ADC in a test experiment. Both data and clock sequences are displayed in the upper traces.

The two input sequences are delayed one with respect to the other in order to emulate 3 different successive possibilities and verify any possible cases:

- The clock bit and the input data bit are both ON: the flip-flop output is always '1' (case (a) in Fig. 6).
- The clock data remains ON while the input data bit goes to '0', then the ADC will do the sampling and the flip-flop output returns to '0' (case (b) in Fig. 6).
- The input bit is back ON but clock pulse is switch OFF: in this situation the ADC sampling operation is halted and the flip-flop remains in the last stored output logic state. In this condition the value of the analogue input signal is irrelevant (case (c) in Fig. 6).

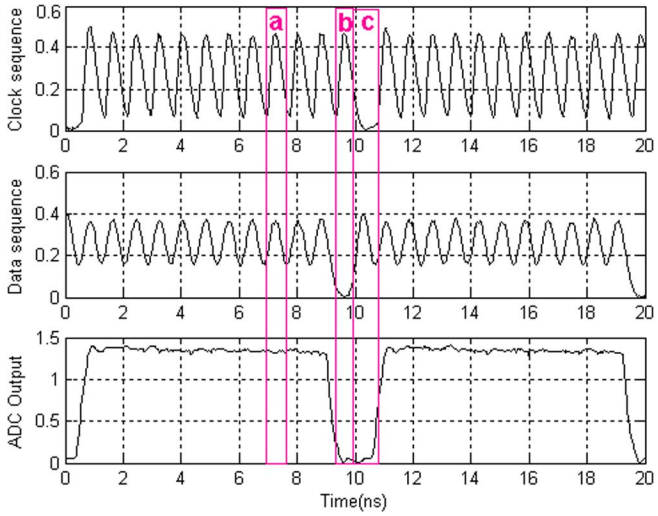


Fig. 6. ADC functionality test with a periodic 13-bit block sequence.

If the routing table is fixed, a logic circuit may be used to produce the required command signal. In dynamic routing, an adaptive algorithm must be performed. The only cost effective and power efficient solution is using an FPGA.

The electronic command signal delivered by the label processing subsystem is used to control the optical switch subsystem. Different electrical voltage levels can be assigned for different label subset bit combinations. A simple solution for providing the different mentioned voltage levels is the utilization of a digital-to-analog converter. DAC5686 is a 16-bit, 500 MSPS, dual-channel digital-to-analog converter manufactured by Texas Instruments.

C. Packet Forwarding

The packet-label swapping, together with the optical spatial switching, constitutes the forwarding operation.

1) Label Swapping: In the MPLS protocol, according to the label look-up table in the label processing subsystem, a new label can be generated and used to modulate a laser beam via an optical modulator. The modulation type can be in either an orthogonal modulation format to the payload's [12] or in series with the payload as suggested in the present architectures.

2) Optical Switch and Contention Resolution: Optical switching can be performed using different technologies based on space, time, wavelength, or code diversity. Packet forwarding based on wavelength switching is very well adapted to the technologies of the proposed architecture. The packet payload is wavelength converted on the basis of the processed label subset and then spatially switched through a wavelength demultiplexer. Optical wavelength converters that utilize nonlinearities in SOAs offer some advantages in terms of integration potential, power consumption, and optical power efficiency [13].

Optical switching in most designs is combined with contention resolution, using multiple fiber delay stages consisting of tunable wavelength converters and banks of fiber delays. Such a scheme has been experimentally presented in [14] and theoretically in [7]. The contention resolution (CR) scheme shown is equivalent in terms of functionality to k parallel Time Slot Interchangers (TSIs), whose inputs correspond to the various outputs of the spatial-switch unit designs to be launched in the same output fiber. According to the architecture of [1], packets at identical wavelength can arrive at these points during overlapping periods of time.

In general, contention resolution for optical packet or burst of packets using programmable delay lines maintains the advantages of lower energy per written/read bit and smaller power dissipation, as compared to electronic buffers, and have been extensively used to form feed-forward or recirculating architectures. In the feed-forward method, packets are fed into fiber delay lines of different lengths and when a burst reaches the output it has to be switched out. In the feedback scheme, a burst may recirculate from the buffer output to the buffer input until contention is resolved and the requested outgoing link is free. The command to set the routing paths inside the contention resolution (setting up the wavelength converters) is provided by a contention control unit, which is informed of the contention by the label-recognition FPGAs that have decoded and process the optical label.

III. All-Optical Packet-Switching System

The second architecture proposal is the all-optical solution displayed in Fig. 7. The synchronization and buffering subsystem is similar to that presented in Section II. The other subsystems are described in the following sections.

A. Label Extraction and Processing

The time-to-wavelength converter is employed once again in order to parallelize the packet label subset. Next, the parallelized bits are amplified and sent to a customized optical decoder module which produces an optical command pulse corresponding to each label subset bit combination.

A decoder is a multiple-input, multiple-output logic circuit that converts parallel coded inputs into coded outputs. It consists of combinational circuits that convert binary information from n-bit coded inputs to 2^n unique outputs. The demonstration of an all-optical 3×8 decoder based on the cross polarization modulation (XPolM) effect in SOA at 10 Gbit/s is presented in [15]. The measured extinction ratio of the output signals is between 7.9 and 12 dB. The design requires only one active optical device per output.

The bit error rate estimated an eye-diagram histogram is 10^{-7} on "1" and 10^{-8} on "0" bits (PRBS $2^{15} - 1$). As each decoder output is zero for seven input bit combinations and one for only one input bit combination, the probability of "0" and "1" bits at each decoder output is 7/8 and 1/8, respectively. Therefore, the bit error rate of our decoder is 2.2×10^{-8} is well adapted to the complete architecture.

B. Packet Forwarding

The packet-forwarding system includes four subsystems, namely: the adaptive wavelength selection, the packet envelope detection, the label stripping and the wavelength conversion, which are all discussed here.

1) Adaptive Wavelength Selection: This unit is required in order to generate or select a wavelength on which the packet payload is to be converted based on the label processed by the decoder unit. One step toward the all-optical architecture of

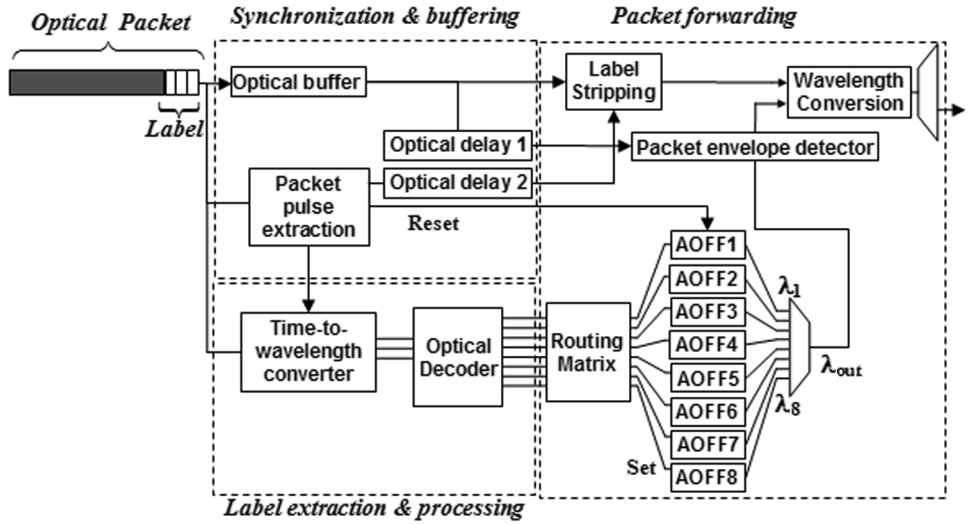


Fig. 7. Schematic representation of an all-optical packet-switching system.

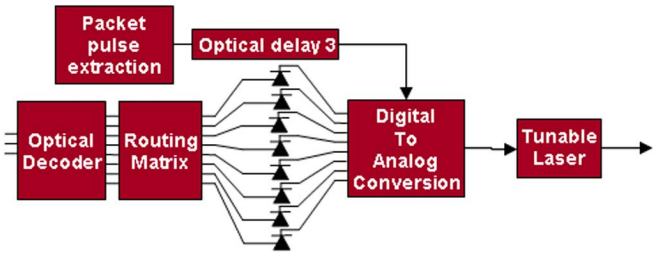


Fig. 8. Adaptive wavelength generator subsystem dedicated to setting up the input wavelength of the wavelength converter as in Fig. 7.

Fig. 7 consists in using an optoelectronic subsystem to emulate the wavelength generator dedicated to setting up the input wavelength of the wavelength converter used for spatially switching the packet payload. This optoelectronic design Fig. 8 has permitted us to fully test the all-optical decoder. The packet pulse extraction output pulse is detected and launched onto the chip-enable input of the digital-to-analog converter (DAC). The chip is therefore active during the time required for the operation i.e., the duration of a packet. The eight outputs of the decoder (shuffled by an active or a passive routing matrix if required) are detected and launched into the DAC inputs which consequently send a leveled signal to the command of the tunable laser. The detected decoder output signals must be greater than the DAC input threshold voltage (e.g. for DAC5686 fabricated by Texas Instruments, the input signal range is [0.1–1.25 V]). A similar wavelength channel selection circuit, which supports 100 wavelength channels spaced by 0.4 nm with a measured switching time of 100 ns, has been proposed in [16]. As in the case of the optoelectronic architecture of Section II, the electronic device can forward information on possible contention to a control unit. In order to provide a reconfigurable packet-switching system, a routing matrix subsystem is proposed. It consists of a series of interconnected elements controlled by the routing plane and is responsible for mapping the incoming packet address to the appropriate outgoing link (look-up table).

An all-optical solution consists in using all-optical flip-flops [1] in order to provide the wavelength selection system displayed in Fig. 7. An optical flip-flop provides two stable wavelengths (λ_{ON} and λ_{OFF}) and thereby is capable of serving as a one bit memory. A flip-flop is controlled by one or two control signals (called set and reset signals). The switching time, the power of the set and reset pulses used to switch the device and the integrability are the key parameters of the optical flip-flops [4]. Each optical flip-flop has two emitting wavelengths, namely λ_{ON} and λ_{OFF}. The λ_{OFF} for all of the flip-flops are identical (e.g. λ_0). It will be filtered out by the demultiplexer (cf Fig. 7). Eight distinct wavelengths $(\lambda_1, \ldots, \lambda_8)$ are chosen for the eight flip-flops' λ_{ON}. In the first step, all of the flip-flops are reset by the packet-pulse extraction. The output pulse of the decoder passes through routing matrix and sets its associated optical flip-flop. Finally, the selected wavelength (λ_{ON}) is launched into the proper input of the multiplexer so as to pass through it to the connected output.

The set and reset pulse-widths are important in this design, which depends on the all-optical flip-flop technology. When the label bits are modulated in RZ format, the set and reset pulse-widths (for instance, $\sim$10 ps in bit rate of 40 Gbit/s) may be insufficient for driving (switching) the flip-flops. Pulsewidth conversion [17] and RZ to NRZ conversion [18] are two of the techniques proposed for all-optical pulse broadening.

2) Packet Envelope Detection: The payload-envelope detection (PED) function is used in the label-erase/rewrite process to precisely locate the associated payload without processing its internal content bits. A new all-optical packet envelope detection based on SOA-MZI gates is proposed; Fig. 9 shows the schematic of this envelope detector.

In order to extract the envelope of an incoming packet, a Fabry-Perot (FP) filter with a free spectral range (FSR) equal to the line rate is used to transform the data packets into clock packets with intense amplitude modulation and duration similar to the corresponding data packets [3]. The output of the filter is then fed into the SOA-MZI gate. By using a single control switching scheme and by biasing the device through the SOAs

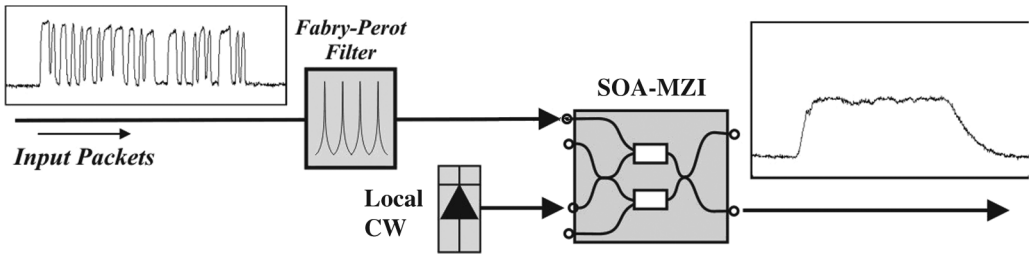


Fig. 9. 10-Gbit/s packet envelope detector using SOA-MZI technique.

currents, the recovery time of the device is increased and as a result, the high frequency modulation harmonics of the signal are suppressed by the SOA-MZI. The output of the device is the recovered packet envelope converted to the local CW wavelength.

By replacing the local CW beam by the output beam of adaptive wavelength selection subsystem (λ_{out} in Fig. 7), a new payload envelope on a packet label-based wavelength will be provided.

3) Packet Label Stripping: Recently, new labeling methods have been proposed whereby new label generation for label swapping in every intermediate network node is not required [19]. The packet end-to-end label consists of multiple local labels. In each intermediate node, a part of this label (associated to the local label) is stripped off and a switching decision is made. This procedure is repeated up to the end of the destination network node. This method can simplify the proposed forwarding architecture.

The contention resolution is somewhat equivalent to that of Section II. However the absence of any electronic subsystem prevents the provision of any information to a potential contention control unit. This has been noticed in [1]. An alternative contention resolution scheme is proposed to the expense of wavelength and time-slot over-use. It must be noted that using a post-switching contention system as described in [1] (with for example a time-slot interchangers device described in Section II-C) rather than feedback loops as in [2] reduces the information required to compute the contention. Arrival time and wavelength of packets are the only required information since the address has been recognized in the previous stage.

IV. Discussion

Both packet-switching systems presented in this paper and illustrated in Figs. 1 and 7 are transparent for the packet payload. The presented schemes have many other benefits, including the following.

- *packet-rate scalability:* The packet bit rate is significant in two places of the switching nodes. Due to the payload transparency, the payload data rate must be considered only at the level of the final wavelength conversion. Fast wavelength conversion (40 Gbit/s) has been demonstrated. For higher rates, other types of spatial switches may be employed since the switching speed is determined only by the packet duration (and not the bit rate). The second implication of the signal rate concerns the label subset used for the switching and is critical only at the input of the time-to-wavelength conversion. (After passing through the time-to-wavelength converter, the bits are parallelized and the initial bit-rate is no longer significant). It can be seen easily that the only modification needed to tune the operation rate of this device is to reduce the dispersion of the dispersive element or the wavelength spacing of the lasers in order to reduce the time difference of the colored pulses as well as to increase the pulse modulation speed. The packet bit-rate variation is not possible in FBG based time-to-wavelength converters.
- *Asynchronous mode operation:* As shown in Fig. 4, the proposed time-to-wavelength converter as well as the other subsystems only needs receiving information on the time of arrival of the label in order to operate properly. This timing information is delivered internally by the packet-pulse extractor. The delay between the intermediate components can be precisely tuned in order to deal with the delay of each operation. Therefore, the packet switching architecture proposed can cope with asynchronous operation and are packet-length independent.
- *Modularity:* Every subsystem presented in Figs. 1 and 7 can be optimized separately. In other words, the realization and the optimization of each subsystem can be done independently.
- *Flexibility:* By increasing the order of the time-to-wavelength converter, the length of the label subset processed may be increased. FWM conversion efficiency for larger wavelength detunings may become critical. Dual pump based FWM methods can be used in order to overcome this problem. On the other hand, the all-optical decoder does not seem to be able to cope with a larger number of bits to process. The optoelectronic solution may be better for such cases.
- *Polarization diversity:* As the input packet-polarization state is unknown, using FWM or XPolM in the time-to-wavelength converter or the optical decoder may become problematic. A solution consists in inserting a polarization insensitive wavelength converter such as the one presented in [20] with a full C-band 40-Gbit/s NRZ operation and polarization insensitive operation of the SOA-MZI wavelength at the input of the switching system in order to set the operational polarization to the desired state.

V. Conclusion

The design and the partial implementation of a packet-routing system are demonstrated in this article. Two solutions for a full "single wavelength label-recognition and packet-forwarding" unit are presented based respectively based on an optoelectronic

architecture and an all-optical one. In both architectures, a label subset is processed in order to route the packet. A time-to-wavelength converter is employed as a serial-to-parallel converter. The slowed-down parallelized label bits are processed either via an electronic subsystem or within an all-optical decoder. The main advantage of these approaches is the ability to route the packets or bursts independently of packet length.

Asynchronous mode functionality of the proposed packet label-processing module depends directly on the performance of the pulse-packet extraction subsystem. Optical integration of the subsystems appears to be possible and will be valuable for reducing cost and enhancing flexibility.

ACKNOWLEDGMENT

The authors participate in the EU FP6 Network of Excellence e-Photon/ONe+ and EU FP7 Network of Excellence BONE.

REFERENCES

[1] F. Ramos, E. Kehayas, J. M. Martinez, R. Clavero, J. Marti, L. Stampoulidis, D. Tsiokos, H. Avramopoulos, J. Zhang, P. V. Holm-Nielsen, N. Chi, P. Jeppesen, N. Yan, I. T. Monroy, A. M. J. Koonen, M. T. Hill, Y. Liu, H. J. S. Dorren, R. V. Caenegem, D. Colle, M. Pickavet, and B. Riposati, "IST-LASAGNE: Towards all-optical label swapping employing optical logic gates and optical flip-flops," *J. Lightw. Technol.*, vol. 23, no. 10, pp. 2993–3011, Oct. 2005.

[2] S. Yao, B. Mukherjee, S. J. Ben Yoo, and S. Dixit, "A unified study of contention-resolution schemes in optical packet-switched network," *J. Lightw. Technol.*, vol. 21, no. 5, pp. 672–683, Mar. 2003.

[3] G. K. Chang, J. Yu, Y. K. Yeo, A. Chowdhury, and Z. Jia, "Enabling technologies for next-generation optical packet-switching networks," *Proc. IEEE*, vol. 94, no. 5, pp. 892–910, May 2006.

[4] H. J. S. Dorren, M. T. Hill, Y. Liu, N. Calabretta, A. Srivatsa, F. M. Huijskens, H. de Waardt, and G. D. Khoe, "Optical packet switching and buffering by using all-optical signal processing methods," *J. Lightw. Technol.*, vol. 21, no. 1, pp. 2–12, Jan. 2003.

[5] M. C. Hauer, J. E. McGeehan, S. Kumar, J. D. Touch, J. Bannister, E. R. Lyons, C. H. Lin, A. A. Au, H. P. Lee, D. S. Starodubov, and A. E. Willner, "Optically assisted internet routing using arrays of novel dynamically reconfigurable FBG-based correlators," *J. Lightw. Technol.*, vol. 21, no. 11, pp. 2765–2778, Nov. 2003.

[6] H. Uenohar, T. Seki, and K. Kobayashi, "High-speed optical packet switch with an optical digital-to-analog conversion-type header processor," *Opt. Rev.*, vol. 11, no. 2, pp. 113–118, 2004.

[7] K. Yiannopoulos, K. Vlachos, and E. Varvarigos, "Multiple-input buffer and shared buffer architectures for optical packet and burst switching networks," *J. Lightw. Technol.*, vol. 25, no. 6, pp. 1379–1389, Jun. 2007.

[8] E. Kehayas, D. Tsiokos, P. Bakopoulos, D. Apostolopoulos, D. Petrantonakis, L. Stampoulidis, A. Poustie, R. McDougall, G. Maxwell, Y. Liu, S. Zhang, H. J. S. Dorren, J. Seoane, P. V. Holm-Nielsen, P. Jeppesen, and H. Avramopoulos, "40-Gb/s all-optical processing systems using hybrid photonic integration technology," *Opt. Expr.*, vol. 13, no. 2, pp. 475–480, Jan. 2005.

[9] H. Harai and M. Murata, "Optical fiber-delay-line buffer management in output-buffered photonic packet switch to support service differentiation," *IEEE J. Select. Areas Commun.*, vol. 24, no. 8, pp. 108–116, Aug. 2006.

[10] R. S. Tucker, K. P. Cheng, and C. J. C. Hasnain, "Slow-light optical buffers: Capabilities and fundamental limitations," *J. Lightw. Technol.*, vol. 23, no. 12, pp. 4046–4066, Dec. 2005.

[11] H. Teimoori, J. D. Topomondzo, C. Ware, and D. Erasme, "All-optical packet-switching decoder design and demonstration at 10 gbit/s," *IEEE Photon. Technol. Lett.*, vol. 19, no. 10, pp. 738–740, May 2007.

[12] K. Vlachos, I. T. Monroy, A. M. J. Koonen, C. Peucheret, and P. Jeppesen, "Stolas: Switching technologies for optical label signals," *IEEE Commun. Mag.*, vol. 41, no. 11, pp. 43–49, Nov. 2003.

[13] Y. Liu, E. Tangdiongga, Z. Li, H. de Waardt, A. M. J. Koonen, G. D. Khoe, X. Shu, I. Bennion, and H. J. S. Dorren, "Error-free 320-Gbit/s all-optical wavelength conversion using a single semiconductor optical amplifier," *J. Lightw. Technol.*, vol. 25, no. 1, pp. 103–108, Jan. 2007.

[14] O. Zouraraki, K. Yiannopoulos, P. Zakynthinos, D. Petrantonakis, E. Varvarigos, A. Poustie, G. Maxwell, and H. Avramopoulos, "Implementation of an all-optical time-slot-interchanger architecture," *IEEE Photon. Technol. Lett.*, vol. 19, no. 17, pp. 1307–1309, Sep. 2007.

[15] H. Teimoori, J. D. Topomondzo, C. Ware, and D. Erasme, "All-optical packet-switching decoder design and demonstration at 10 gbit/s," *IEEE Photon. Technol. Lett.*, vol. 19, no. 10, pp. 738–740, May 2007.

[16] C.-K. Chan, K. L. Sherman, and M. Zirngib, "A fast 100-channel wavelength-tunable transmitter for optical packet switching," *IEEE Photon. Technol. Lett.*, vol. 13, no. 7, pp. 729–731, Jul. 2001.

[17] G. A. Rauschenbach, K. L. Hall, J. C. Livas, and G. Raybon, "All-optical pulse width and wavelength conversion at 10 Gb/s using a nonlinear optical loop mirror," *IEEE Photon. Technol. Lett.*, vol. 6, no. 9, pp. 1130–1132, Sep. 1994.

[18] T. G. Silveira, A. Teixeira, G. T. Beleffi, D. Forin, P. Monteiro, H. Furukawa, and N. Wada, "All-optical conversion from RZ to NRZ using gain-clamped SOA," *IEEE Photon. Technol. Lett.*, vol. 19, no. 6, pp. 357–359, Mar. 2007.

[19] E. Kehayas, K. Vyrsokinos, L. Stampoulidis, K. Christodoulopoulos, K. Vlachos, and H. Avramopoulos, "Artemis: 40-Gb/s all-optical self-routing node and network architecture employing asynchronous bit and packet-level optical signal processing," *J. Lightw. Technol.*, vol. 24, no. 8, pp. 2996–2977, Aug. 2006.

[20] T. Hatta, T. Miyahara, Y. Miyazaki, K. Takagi, K. Matsumoto, T. Aoyagi, K. Motoshima, K. Mishina, A. Maruta, and K. Kitayama, "Polarization-insensitive monolithic 40-gbps SOA-MZI wavelength converter with narrow active waveguides," *IEEE J. Sel. Topics Quantum Electron.*, vol. 13, no. 1, pp. 32–39, Jan.–Feb. 2007.

Hassan Teimoori was born in Mashhad, Iran, in 1978. He received the B.S. degree in electrical engineering from Ferdowsi University, Mashhad, in 2000, the M.S. degree in telecommunication engineering from Tehran University, Tehran, Iran, in 2003, the M.S. degree in optics and microwaves from the École Nationale Polytechnique de Grenoble, Grenoble, France, in 2004, and the Ph.D. degree, specializing in optical packet-switching networks, from the École Nationale Supérieure des Télécommunications, Paris, France, in 2007.

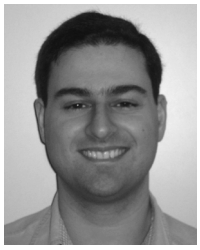
He is currently with Centre for Research in Photonics, School of Information Technology and Engineering (SITE), University of Ottawa, Ottawa, Canada.

Dimitrios Apostolopoulos, photograph and biography not available at the time of publication.

Kyriakos G. Vlachos (S'00–M'02) received the Dipl.-Ing. and Ph.D. degrees in electrical and computer engineering from the National University of Athens (NTUA), Athens, Greece, in 1998 and 2001, respectively.

From 1997 to 2001, he was a Senior Research Associate in the Photonics Communications Research Laboratory (ICCS/NTUA). In April 2001, he joined Bell Laboratories, Lucent Technologies, working on behalf of the Applied Photonics Group. Since 2005, he has been a faculty member in the Computer Engineering and Informatics Department, University of Patras, Patras, Greece. His research interests are in the areas of high-speed protocols and technologies for broadband, high-speed networks, optical packet/burst switching, and grid networks. He has participated in various research projects funded by the European Commission (IST-STOLAS, IST-PRO3, ESPRITDOALL, e-photon/ONe+ and IST-PHOSPHOROUS). He is the (co)-author of more than 70 journal and conference publications and holds five patents.

Dr. Vlachos is a member of the Technical Chamber of Greece.



Cédric Ware was born in Paris, France, on January 24, 1977. He received the B.Sc. degree in computer science and the M.Sc. degree in physics from the École Normale Supérieure, Paris, and the Université Paris 6 and 7, Paris, in 1996, the Engineering degree from the École Nationale Supérieure des Télécommunications, Paris, in 1998, where he also received the Ph.D. degree, specializing in optoelectronic clock recovery, in 2003.

Since 1998, he has been with the Department of Communications and Electronics, École Nationale Supérieure des Télécommunications, as an Assistant Professor, and since 2007 as an Associate Professor. His current research activities include optical signal processing for use in optical communications networks, notably clock recovery, packet label recognition, and optical code division multiple access. He is a National Delegate for the European Cooperation in the Field of Scientific and Technical Research (COST) 288 on nanoscale and ultrafast photonics and the Vice Chairman of its working group on photonics devices. He also participates in COST 291 on digital optical networks and the European Networks of Excellence BONE and EuroFOS.

Dr. Ware is a member of the Optical Society of America.

Dimitrios Petrantonakis, photograph and biography not available at the time of publication.

Leontios Stampoulidis, photograph and biography not available at the time of publication.

Hercules Avramopoulos, photograph and biography not available at the time of publication.

Didier Erasme was born in Paris, France, in 1960. He received the Dipl. Ing. degree in physical engineering from the Ecole Nationale Supérieure d'Ingénieurs Electriciens de Grenoble (INPG), Grenoble, France, in 1983 and the Ph.D. degree in LiNbO3 high-frequency integrated-optic modulators from the Electrical and Electronic Engineering Department, University College London (UCL), London, U.K., in 1987. In 1995, he received the "Habilitation à diriger des recherches".

After two years of postdoctoral work on electrooptic sampling of GaAs-integrated circuits at UCL, he joined the Ecole Nationale Supérieure des Télécommunications (Télécom ParisTech) in 1990 as an Associate Professor in optoelectronics. He spent a six-month sabbatical at Delft University, Delft, The Netherlands. Since 1998, he has been a Full Professor at Télécom ParisTech. His current research interests are in the area of new optical functions for telecommunication optical systems and networks. He has developed a strong interest in semiconductor laser amplifiers and other nonlinear optical devices for applications in all-optical signal processing. Applications range from ultra high-speed clock recovery and OTDM demultiplexing to the realization of subsystems dedicated to optical packet-switching nodes. He is the author and co-author of more than 70 publications and communications in international journals and conferences. He has participated in the European programmes OPTIMIST and BREAD dedicated to the road-mapping of European Broadband-for-all activities in Europe and to the European Network of Excellence ePhoton/ONe and now BONE and EUROFOS.