Optically-Addressable Packet Timeslot Interchanger Using a Quadruple Switch Array

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Abstract: We propose and demonstrate a wavelength converter-based Time-Slot-Interchanger architecture consisting of cascaded programmable delay stages. It uses an integrated quadruple switch array of HMZI switches and operated error-free with 10 Gb/s NRZ packets.

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1. Introduction

Optical packet switched (OPS) networks are expected to enable the most efficient exploitation of the existing transmission bandwidth [1]. A key issue in OPS networks is the availability of optical storage elements that will allow for contention resolution in the network nodes. A practical and simple means of storing optical packets is the use of Time-slot-interchangers (TSIs); optical packets that contend at the node output are directed to the TSI, where they interchange their time-slots with time-slots of non-contending packets. TSIs are implemented in architectures that incorporate feed-forward and feedback delay line setups [2]. Feedback setups offer TSI capabilities between time-slots that are theoretically infinitely long apart, however they practically suffer from loss of synchronization. On the other hand, feed-forward setups are more practical approach to TSI implementation, since they are simpler to synchronize. Recent studies indicate that statistically multiplexed optical networks will be capable of providing high network utilization even with minimal buffering, provided that traffic engineering is performed at the network ingress nodes [3]. Thus, there will be no real need for large TSI spans.

In this paper, we propose and experimentally demonstrate a Tunable Wavelength Converter (TWC) based feed-forward delay line TSI architecture for limited interchanging spans, using the first integrated quadruple SOA-MZI switch array. The architecture is implemented as a cascade of programmable delay stages engineered so that their number, thus the total number of TWCs, grows optimally with the interchanged time-slots. It enables minimization of delay stages, by taking full advantage of the TWC's WDM parallelism. The experimental demonstration of the scheme shows error-free interchanging of four time-slots at 10 Gbps for three programmable delay stages.

2. Concept and Experimental Setup

The structure of the programmable delay stages that comprise the TSI is presented in Fig. 1(a). Each stage consists of a tunable wavelength converter (TWC) that provides *w* separate wavelengths at its output, and a bank of *w* parallel delay lines, one per wavelength. The TWC assigns the incoming packets with wavelengths and each packet accesses the assigned output time-slot by propagating through the delay line that corresponds to its wavelength. We will determine the delays that are introduced at each stage from the time-slot transition graph (TTG) of the TSI architecture [4], which is shown in Fig. 1(b) for stage 0. The TTG consists of nodes located at columns and rows; columns *i* and *i+1* represent the inputs and outputs, respectively, of TSI stage *i*, while rows account for the time-slots. Nodes that are located at the input of stage *i* connect to nodes at the stage output with time transitions, which are presented as straight lines on the TTG. Time transitions inside the TSI stage *i* correspond to the packet accessing a delay line, and as a result time transitions may not access output nodes that are located at previous time-slots. We assume that each packet occupies at most one time-slot.

We determine time transitions, or equivalently the delay times at each stage, so that they construct a $\log_n$-Benes interconnection network on the TTG. The $\log_n$-Benes network is illustrated in Fig. 1(c) and is derived from the $\log_2$-Benes after replacing the 2x2 switches with *nxn* crossbars. We evaluate the size of the crossbars *n* in Fig. 1(b) as

$$n = w - n + 1 \Leftrightarrow n = \left\lfloor \frac{w+1}{2} \right\rfloor, \qquad (1)$$

with $\lfloor x \rfloor$ denoting the integer part of x. Eq. (2) is due to the fact that only time-slots {n,..,w} may be assigned to all packets that have arrived within {1,…n}.

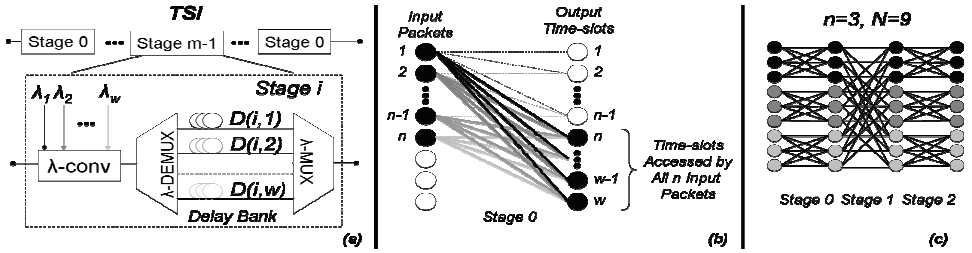

Figure 1: (a) Programmable delay stage structure, (b) Formation of the *nxn* crossbar on the TTG, (c) The $\log_n$-Benes network

We interconnect the crossbars to form the $\log_n$-Benes network as in fig 1(c). At each stage i of the $\log_n$-Benes network, the crossbars interconnect time-slots that are located n^i positions apart, thus the time delays equal

$$D(i, j) = j \cdot n^i, \quad i = 0,...,m-1, \quad j = 0,...,w-1. \tag{2}$$

The purpose of constructing the $\log_n$-Benes network is many-fold. First, it requires a minimum number of serially connected stages, as compared to other interconnection networks, that equals

$$s = 2 \cdot m - 1 = 2 \cdot \lceil \log_n N \rceil - 1, \tag{3}$$

where N is the number of interchanged packets. Consequently the architecture requires the minimum number of stages, thus wavelength converters and accompanying current supplies and cooling equipment, for a given N. Eq. (3) also shows that it is possible to reduce the required number of stages at the expense of increasing n. As a result, a small increase in the number of available wavelengths causes a substantial reduction in the number of cascaded TWCs. In addition, the Benes network is re-arrangably non-blocking and this property ensures that by properly setting the internal wavelengths two packets never arrive simultaneously at the TWCs inputs. Therefore the TSI is capable of performing without internal collisions for up to N successive packets, irrespective of the packet order. Finally, setting the internal wavelengths of the TSI corresponds is equivalent to finding a collision free path within the Benes network, which is a well studied problem.

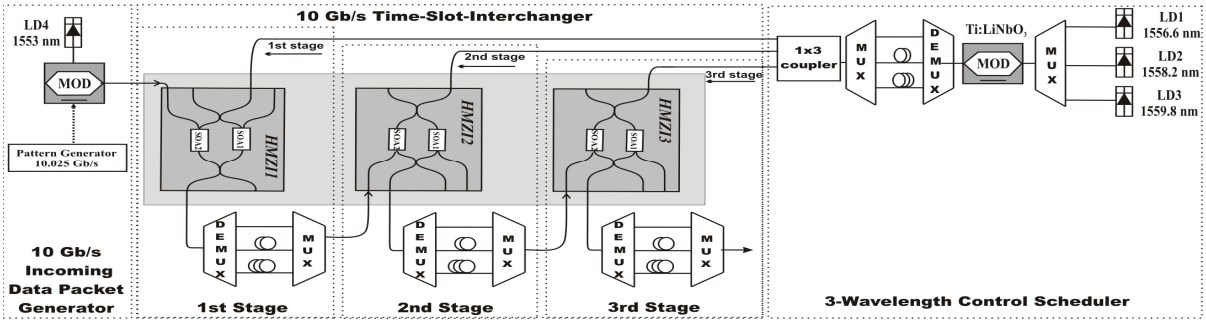

Figure 2: Experimental set-up of the TSI architecture with the quadruple switch array.

The experimental setup of the TSI architecture corresponds to w=3 and s=3 and is shown in Fig. 2. It consists of the three-Wavelength Control Scheduler, the 10 Gb/s NRZ Data Packet Generator and the 10 Gb/s TSI circuit implemented by a quadruple SOA-MZI array. The Wavelength Control Scheduler involves three CW signals (1546.6 nm, 1548.2 nm and 1559.8 nm) which are multiplexed and modulated into CW packets that coincide in the time domain. The CW packets are introduced into a wavelength dependent delay configuration comprising Demux/Mux-es and fiber segments with lengths that correspond to zero, one and two timeslots, respectively. A sequence of three consecutive CW packets of same-length and different-wavelength is thus obtained at the output of the Demux. The CW packet sequence is then split into three parts which form the input signals of the three stages in our circuit. The 10 Gb/s Incoming Data Packet Generator employs a 1553 nm laser and a modulator to generate a sequence of 10.025 Gb/s NRZ data packets which are injected into the first stage of the TSI. The TSI stages deploy a packaged HMZI, shown in Fig. 3(f), and a Demux/Mux based programmable delay bank. The HMZI operates as a wavelength converter, assigning each data packet that appears at its control port with one of the three input wavelengths, while the delay bank is used to delay each incoming data packet according to the wavelength it has

been assigned. As a result, incoming packets are interchanged at the stage output based upon the wavelength assignment procedure. The wavelength-converted packets at output of each stage are fed to the control port of the next stage HMZI in a counter-propagating control/input signal fashion except for the first stage.

3. Results and Discussion

Figure 3 illustrates the incoming packets in each stage of the TSI circuit. In particular, figure 3(a) shows the input signal, consisting of four, 40-bits long timeslots. The first three timeslots accommodate 25-bits long, synchronous data packets at 10 Gb/s, followed by 15-bits time interval between them while the fourth one is empty. Figure 3(b) depicts the output of the TSI's first stage. Packets A and B are converted to different wavelengths, corresponding to appropriate delay lines, so as to exchange their positions while Packet C remains in the same timeslot. Figure 3(c) presents the second stage of the TSI circuit. In this stage, Packet A occupies the same time slot, while Packet B and C interchange their positions, using the same, wavelength-assigning procedure described above. Figure 3(d) shows the output of the final stage of our circuit. Packets A and B interchange their timeslots position, while Packet C exits the circuit without experiencing any delay.

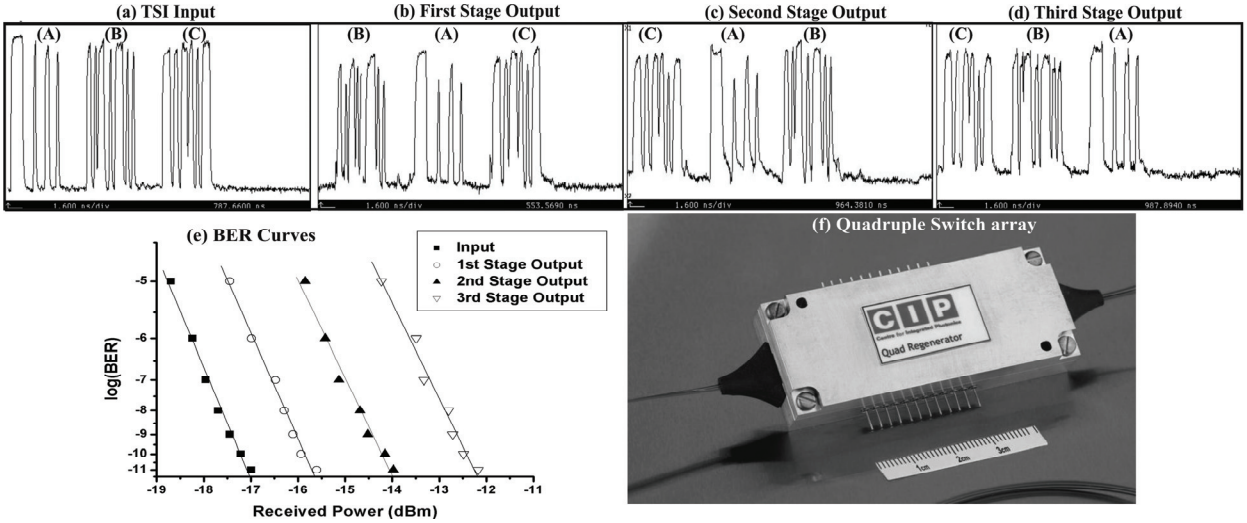

Figure 3: Pictures of (a) the input data packets (b) first stage output, (c) second stage output , (d) third stage output., (e) BER curves and (f) the quadruple HMZI switch. The time scale for the traces is 1.6 ns/div.

Figure 3(e) demonstrates the BER measurements obtained at the output of each stage. Error-free operation was achieved with power penalties of 1.4 dB, 3 dB and 4.8 dB after the first, second and third stages, with respect to the input signal. With our algorithm, the number of interchanging timeslots scales well. Assuming that the TSI is built with 3 stages so as to avoid signal degradation, by using 3 λ's it provides 4 interchangeable timeslots, with 5 λ's it provides 8 timeslots. With 3 stages and a modest number of 11 λ's, the TSI provides 64 interchangeable timeslots which provides adequate buffering for OPS networks.

4. Conclusion

We presented an optically-addressable TSI architecture using a quadruple switch array and feed-forward delay line setups. Error free operation was demonstrated at each stage of our circuit, exploiting integration, programmability and expandability which contribute to an efficient contention resolution scheme in OPS networks.

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Acknowledgments

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